REMARKS

In the Office Action, the Examiner noted that claims 1, 3-23 are pending in the application. The Examiner rejected claims 1 and 3-23. In view of the above amendments and the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in condition for allowance.

I. Rejection of Claims Under 35 U.S.C. §102

A. Claims 1, 4, 6-7, 22 and 23

The Examiner rejected claims 1, 4, 6-7, 22 and 23 as being anticipated by Desai (United States patent 6,288,656, issued September 11, 2001). Claim 7 has been canceled without prejudice. The rejection is respectfully traversed.

More specifically, the Examiner stated that Desai discloses a first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data (see Fig. 7, Channel 1, serial data RDX1 and block 706 "Clock Recovery", outputting a first recovered clock from the first serial data RDX1, column 1, lines 7-8 where the invention relates to a transceiver, column 5, lines 45-59). The Examiner further cited the same section in Desai for the teaching of a second clock data recovery circuitry for receiving second serial data. The Examiner then stated that Desai discloses a transceiver that provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a circuit portion of the transceiver (Fig. 7 circuit portion to the right of FF block 704, the recovered clocks of channels 1, 2 and one of the channel word clock(s) corresponding to the reference clock that is used to deserialize the data into parallel data words, (see column 4, lines 32-34), RXD1, RXD2 serial streams)). The Examiner then concluded that Desai anticipates Applicants' invention as recited in claims 1, 4, 6-7, 22 and 23.

Desai teaches a deserializer for generating parallel data. More specifically, Desai discloses a receive deserializer which regenerates parallel data words that have been broken into smaller data words and serially transmitted over multiple data channels that uses an external state machine to shift word clocks with respect to data

until the output of the channel last to receive a predefined data reference pattern is framed and provides storage to hold data for the channels which receive the reference pattern earlier. (See Desai, Abstract)

Desai, however, does not teach each and every element of Applicants' independent claims 1, 6, 22 and 23. Namely, Desai does not teach or suggest a method that chooses among a first recovered clock signal, a second recovered clock signal and a reference clock signal to perform processing functions as positively claimed by the Applicants.

In one embodiment, Applicants' invention discloses an approach where the logic is provided with a first recovered clock signal, a second recovered clock signal and a reference clock signal, from which the logic is able to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal. (See, e.g., Applicants' Specification, paragraphs [0051], [0069]; FIGs. 5, 6, 7, 8, and 12, where the logic is able to choose among the recovered signals and the reference signal). In contrast, Desai at best might teach a plurality of recovered clock signals, but there is no teaching in Desai that the logic has the ability to choose among the plurality of recovered clock signals. For example, FIG. 7 of Desai clearly shows that each of the plurality of recovered clock signals is provided to separate CLKGEN 710. There is no teaching that each separate CLKGEN is able to choose a different clock signal among a plurality of available clock signals. Thus, Desai fails to teach or suggest Applicants' invention where the logic is able to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal.

Furthermore, the Examiner alleged that the channel word clock of Desai is a reference clock signal. However, it is clear that Desai's channel word clock is a clock signal that is based on the recovered clock signals (see e.g., Desai, FIG. 7). As such, at best, Desai's channel word clock might be a modified recovered clock signal and not a reference clock signal.

Since Desai does not teach the ability to allow the logic to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal, Desai does not teach each and every element of Applicants' independent

claims 1, 6, 22 and 23. Accordingly, Desai does not anticipate Applicants' invention recited in claims 1, 6, 22 and 23.

Furthermore, claim 4 depends from claim 1 and recites additional features therefor. Since Desai does not anticipate Applicants' invention as recited in claim 1, dependent claim 4 is also not anticipated and is allowable. Therefore, the Applicants contend that claims 1, 4, 6, 22 and 23 are not anticipated by Desai and, as such, fully satisfy the requirements of 35 U.S.C. §102.

B. Claims 1, 4-7, and 10-23

The Examiner rejected claims 1, 4-7, and 10-23 as being anticipated by Mann (United States patent 5,251,210, issued October 5, 1993). Claims 7 and 17 have been canceled without prejudice. The rejection is respectfully traversed.

More specifically, the Examiner stated that Mann discloses a first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data (Fig. 7, see Channel 1, blocks 260, 250, see column 14, lines 28-39, for serial data streams, see column 6, lines 39-43). The Examiner further cited the same section in Mann for the teaching of a second clock data recovery circuitry for receiving second serial data. The Examiner then stated that Mann discloses a transceiver that provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a circuit portion of the transceiver (see column 1, lines 9-11, transmitting/receiving communication system (transceiver) and Fig. 7 (the receiver side)). The Examiner then concluded that Mann anticipates Applicants' invention as recited in claims 1, 4-7, and 10-23.

Mann teaches a method for transforming low bandwidth telecommunications channels into a high bandwidth telecommunication channel. More specifically, Mann teaches that low bandwidth telecommunications channels are transformed into a high bandwidth telecommunications channel by determining the relative transmission delays among a plurality of relatively low bandwidth channels which are to be combined into a relatively high bandwidth communications channel. The transmission time delay across the plurality of low bandwidth channels is then equalized so that the

time delay equalized low bandwidth channels combine to effectively form a single high bandwidth channel. (See Mann, Abstract)

Mann, however, does not teach each and every element of Applicants' independent claims 1, 6, 10, 14, 19, 22 and 23. Namely, Mann does not teach or suggest a method that chooses among a first recovered clock signal, a second recovered clock signal and a reference clock signal to perform processing functions as positively claimed by the Applicants.

As discussed above, in one embodiment, Applicants' invention discloses an approach where the logic is provided with a first recovered clock signal, a second recovered clock signal and a reference clock signal, from which the logic is able to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal. In contrast, Mann at best might teach a plurality of recovered clock signals, but there is no teaching in Mann that the logic has the ability to choose among the plurality of recovered clock signals. For example, FIG. 7 of Mann clearly shows that each of the plurality of recovered clock signals is provided to separate FIFO 210 which in turn serves separate Alignment & Alignment monitor pattern Detector 220. There is no teaching that each separate FIFO is able to choose a different clock signal among a plurality of available clock signals. Thus, Mann fails to teach or suggest Applicants' invention where the logic is able to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal.

Furthermore, the Examiner alleged that the RxCLK of Mann is a reference clock signal. However, it is clear that Mann's RxCLK is a clock signal that is based on the combined payload data rate of the individual T1 data channels of the carrier network, i.e., RxCLK = N x (data channel rate – alignment monitor pattern data rate). (see e.g., Mann, Column 15, lines 34-38). As such, Mann's RxCLK is not a reference clock signal.

Since Mann does not teach the ability to allow the logic to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal, Mann does not teach each and every element of Applicants' independent

claims 1, 6, 10, 14, 19, 22 and 23. Accordingly, Mann does not anticipate Applicants' invention recited in claims 1, 6, 10, 14, 19, 22 and 23.

Furthermore, claims 4-5, 11-13, 15-16, 18, and 20-21 depend from claims 1, 6, 10, 14, and 19, respectively and recite additional features therefor. Since Mann does not anticipate Applicants' invention as recited in claims 1, 6, 10, 14, 19, 22 and 23, dependent claims 4-5, 11-13, 15-16, 18, and 20-21 are also not anticipated and are allowable. Therefore, the Applicants contend that claims 1, 4-6, 10-16, and 18-23 are not anticipated by Mann and, as such, fully satisfy the requirements of 35 U.S.C. §102.

C. Claims 8, 9, 22, and 23

The Examiner rejected claims 8, 9, 22, and 23 as being anticipated by Ziegler (United States patent publication 2003/0112798, published June 19, 2003). The rejection is respectfully traversed.

More specifically, the Examiner stated that Ziegler discloses a circuitry for receiving a plurality of input serial data streams and that clock data recovery circuitry recovers a corresponding plurality of recovered clocks. Finally, the Examiner stated that Ziegler discloses logic that provides each received input serial data stream to an outgoing transmit block based upon each of the corresponding recovered clocks.

Ziegler teaches a data communication method. More specifically, Ziegler teaches a method of communicating a plurality of parallel data packets from a first data parallel bus to a second parallel data bus. (See Ziegler, Abstract).

Ziegler, however, does not teach each and every element of Applicants' independent claims 8, 22 and 23. Namely, Ziegler does not teach or suggest a method that chooses among a first recovered clock signal, a second recovered clock signal and a reference clock signal to perform processing functions as positively claimed by the Applicants.

As discussed above, in one embodiment, Applicants' invention discloses an approach where the logic is provided with a first recovered clock signal, a second recovered clock signal and a reference clock signal, from which the logic is able to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal. In contrast, Ziegler at best might teach a single recovered

clock signal and a reference clock signal, but there is no teaching in Ziegler that the logic has the ability to choose among a plurality of recovered clock signals. For example, FIG. 3 of Ziegler clearly shows that each of the plurality of recovered clock signals is provided to a separate logic (312, or 332) and to a separate FIFO (314, or 334). There is no teaching by Ziegler that each separate logic or FIFO is able to choose a different recovered clock signal among a plurality of recovered clock signals. Thus, Ziegler fails to teach or suggest Applicants' invention where the logic is able to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal.

Since Ziegler does not teach the ability to allow the logic to choose among the first recovered clock signal, the second recovered clock signal and the reference clock signal, Ziegler does not teach each and every element of Applicants' independent claims 8, 22 and 23. Accordingly, Ziegler does not anticipate Applicants' invention recited in claims 8, 22 and 23.

Furthermore, claim 9 depends from claim 8 and recites additional features therefor. Since Ziegler does not anticipate Applicants' invention as recited in claim 8, dependent claim 9 is also not anticipated and is allowable. Therefore, the Applicants contend that claims 8-9, 22 and 23 are not anticipated by Ziegler and, as such, fully satisfy the requirements of 35 U.S.C. §102.

II. Rejection Of Claims Under 35 U.S.C. §103

A. Claim 6

The Examiner rejected claim 6 as being unpatentable over Ducaroir (US Patent application 2001/0043648. The rejection is respectfully traversed.

More specifically, the Examiner conceded that Ducaroir does not teach a second circuitry for generating and providing a reference clock signal. However, the Examiner alleged that providing a reference clock signal is known in the art (Official Notice).

Applicants respectfully disagree and challenge the Examiner's taking of the Official Notice. Applicants respectfully request that the Examiner provides the necessary support for taking the Official Notice.

Furthermore, Ducaroir does not teach or suggest a method that chooses among a first recovered clock signal, a second recovered clock signal and a reference clock signal to perform processing functions as positively claimed by the Applicants.

Therefore, Applicants contend that claim 6 is patentable over the combination of Ducaroir and Official Notice and, as such, fully satisfies the requirements of 35 U.S.C. §103.

B. Claim 3

The Examiner rejected claim 3 as being unpatentable over Desai in view of in view of Tang (US Publication No. 2002/0075981). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Desai does not teach a delay locked loop circuitry. The Examiner stated, however, that Tang teaches a delay locked loop circuitry.

As discussed above, Desai does not teach or suggest a method that chooses among a first recovered clock signal, a second recovered clock signal and a reference clock signal to perform processing functions as positively claimed by the Applicants. This deficiency is not bridged by the teaching of Tang.

Therefore, Applicants contend that claim 3 is patentable over the combination of Desai and Tang and, as such, fully satisfies the requirements of 35 U.S.C. §103.

C. Claim 3

The Examiner rejected claim 3 as being unpatentable over Mann in view of in view of Tang. The rejection is respectfully traversed.

More specifically, the Examiner conceded that Mann does not teach a delay locked loop circuitry. The Examiner stated, however, that Tang teaches a delay locked loop circuitry.

As discussed above, Mann does not teach or suggest a method that chooses among a first recovered clock signal, a second recovered clock signal and a reference clock signal to perform processing functions as positively claimed by the Applicants. This deficiency is not bridged by the teaching of Tang.

Therefore, Applicants contend that claim 3 is patentable over the combination of Mann and Tang and, as such, fully satisfies the requirements of 35 U.S.C. §103.

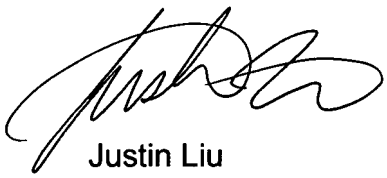
CONCLUSION

Thus, the Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Justin Liu at 408-879-4641 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

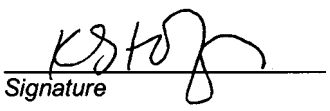
Respectfully submitted,



Justin Liu
Attorney for Applicants
Reg. No. 51959

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 12, 2007.

Katherine Stofer
Name



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